

**Notice of References Cited**

Application/Control No.

10/009,979

Applicant(s)/Patent Under  
Reexamination  
DENK, GEORG

Examiner

A. M. Thompson

Art Unit

2825

Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,539,346	03-2003	Chinosi et al.	703/15
	B	US-6,490,546	12-2002	Kimmel et al.	703/14
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	H. Warmers et al., Switch-Level Timing Models in the MOS Simulator BRASIL, Proceedings of the European Design Automatic Conference, pages 568 -572, March 1990.
	V	U. Bretthauer et al., BRASIL: The Braunschweig Mixed-Mode-Simulator for Integrated Circuits, Proceedings of the Conference with EURO-VHDL '96 and Exhibition on European Design Automation, pages 10-14, September 1996.
	W	G. Droge et al., EASY - A System for Computer-Aided Examination of Analog Circuits, Proceedings of Design, Automation and Test in Europe, pages 644-648, February 1998.
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.